What is claimed is:

[Claim 1] 1. A delay lock loop circuit for delaying a reference clock to lock a delayed clock, the delay lock loop circuit comprising:

a clock divider for dividing a frequency of the reference clock by N to generate a frequency-divided clock;

a programmable delay circuit electrically coupled to the clock divider, the programmable delay circuit for delaying the frequency-divided clock to generate the delayed clock;

a 180° phase detector electrically coupled to the programmable delay circuit, the 180° phase detector for detecting a phase change of the delayed clock; and

a delay lock loop controller electrically coupled to the programmable delay circuit and the 180° phase detector, the delay lock loop controller for programming the programmable delay circuit to lock the delayed clock according to the phase change.

[Claim 2] 2. The delay lock loop circuit of claim 1 further comprising a multiplexer electrically coupled to the clock divider and the reference clock, wherein the multiplexer sends either the reference clock or the frequency-divided clock as the driving clock to the 180° phase detector.

[Claim 3] 3. The delay lock loop circuit of claim 2 wherein if the driving clock is the reference clock, the 180° phase detector is triggered once every N cycles of the reference clock, and if the driving clock is the frequency-divided clock, the 180° phase detector is triggered once each cycle of the frequency-divided clock.

[Claim 4] 4. The delay lock loop circuit of claim 1 wherein a driving clock of the 180° phase detector is the frequency-divided clock.

[Claim 5] 5. The delay lock loop circuit of claim 4 wherein the 180° phase detector is triggered once each cycle of the frequency-divided clock.

[Claim 6] 6. The delay lock loop circuit of claim 1 wherein a driving clock of the 180° phase detector is the reference clock.

[Claim 7] 7. The delay lock loop circuit of claim 6 wherein the 180° phase detector is triggered once every N cycles of the reference clock.

[Claim 8] 8. A delay lock loop circuit for delaying a reference clock to lock a frequency-divided clock, the delay lock loop circuit comprising:

a programmable delay circuit for delaying the reference clock to generate a delayed clock;

a clock divider electrically coupled to the programmable delay circuit, the clock divider for dividing a frequency of the delayed clock by N to generate a frequency-divided clock;

a 180° phase detector electrically coupled to the clock divider, the 180° phase detector for detecting a phase change of the frequency-divided clock; and

a delay lock loop controller electrically coupled to the programmable delay circuit and the 180° phase detector, the delay lock loop controller for programming the programmable delay circuit to lock the frequency-divided clock according to the phase change.

[Claim 9] 9. The delay lock loop circuit of claim 8 wherein a driving clock of the 180° phase detector is the reference clock.

[Claim 10] 10. The delay lock loop circuit of claim 9 wherein the 180° phase detector is triggered once every N cycles of the reference clock.

[Claim 11] 11. A method for delaying a reference clock to lock a delayed clock, the method comprising:

dividing a frequency of a reference clock by N to generate a frequency-divided clock;

delaying the frequency-divided clock by an amount of delay to generate the delayed clock;

providing a 180° phase detector, and utilizing the 180° phase detector for detecting a phase change of the delayed clock; and

programming the amount of delay for locking the delayed clock according to the phase change.

[Claim 12] 12. The method of claim 11 further comprising selecting the reference clock or the frequency-divided clock to be a driving clock of the 180° phase detector.

[Claim 13] 13. The method of claim 12 wherein if the driving clock is the reference clock, the 180° phase detector is triggered once every N cycles of the reference clock, and if the driving clock is the frequency-divided clock, the 180° phase detector is triggered once each cycle of the frequency-divided clock.

[Claim 14] 14. The method of claim 11 wherein a driving clock of the 180° phase detector is the frequency-divided clock.

[Claim 15] 15. The method of claim 14 wherein the 180° phase detector is triggered once each cycle of the frequency-divided clock.

[Claim 16] 16. The method of claim 11 wherein a driving clock of the 180° phase detector is the reference clock.

[Claim 17] 17. The method of claim 16 wherein the 180° phase detector is triggered once every N cycles of the reference clock.

[Claim 18] 18. A method for delaying a reference clock to lock a frequency-divided clock, the method comprising:

delaying a reference clock by an amount of delay to generate a delayed clock;

dividing a frequency of the delayed clock by N to generate the frequency-divided clock;

providing a 180° phase detector, and utilizing the 180° phase detector for detecting a phase change of the frequency-divided clock; and

programming the amount of delay for locking the frequency-divided clock according to the phase change.

[Claim 19] 19. The method of claim 18 wherein a driving clock of the 180° phase detector is the reference clock.

[Claim 20] 20. The method claim 19 wherein the 180° phase detector is triggered once every N cycles of the reference clock.